## REMARKS

Applicants have amended claim 1 in response to the Examiner's rejection under 35 USC section 112, second paragraph. Applicants submit that the modified claim 1 comports with all of the requirements of section 112 and accordingly, Applicants request that the Examiner withdraw the rejections under section 112.

Applicants respectfully request reconsideration of the prior art rejections set forth by the Examiner under 35 USC sections 102 and 103. Applicants respectfully submit that the prior art references of record, whether considered alone or in combination fail to either teach or suggest Applicants presently claimed invention. Applicant notes that the present invention is directed to an improved semiconductor product wherein one or more chip devices are secured to one another via a resin that covers side surfaces and a side opposite the electrodes of the chip.

Advantageously, by selecting only non-defective chip members and securing the non-defective chips via the specified resin to form a pseudo-wafer of non-defective chips, the non-defective chips can be further processed in order to achieve significant cost savings by eliminating the need to further process defective chips. This provides a substantial economic advantage. The independent claims specify the state of the device after the further processed chips have been cut from the wafer thus leaving cut substantially vertical side walls of protective material at the sides of the further processed chip members.

The art of record fails to provide any teaching or suggestion regarding this advance in the art. More specifically, Applicants note that the primary Corisis reference, United States

patent number 5,956,236 is merely directed to a plastic foam material 14b that is used to secure package members 12. There is simply no teaching or suggestion whatsoever regarding the specified chips wherein protective material adjacent to side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip. The high polystyrene foam of Corisis is probably molded and there is simply no teaching or suggestion regarding the claimed cut or diced vertical side walls of protective material.

None of the references of record teach or suggest Applicants claimed advance in the art.

In light of the foregoing, Applicant request that the Examiner now allow all claims in the application.

Respectfully submitted,

Date: 11/19/04

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## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail on 11/19/04 in an envelope addressed to:

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